REMARKS

Claims 1-16 are pending in the application. Claims 1-16 are rejected.

Claim Objections

The independent claims have been amended to clarify "that is included" is referring to "the argument being included." Claims 1, 2, 15 and 16 are amended for clarity.

The Office Action objects to the specification as not clearly defining the purpose of the "argument" and the purpose of the invalid bit.

"Argument":

Applicant's use of the term "argument" is not as in a noun sense, such as "A discussion in which reasons are advanced against some proposal," but applicant's uses the "argument" as a variable. As a variable or "argument" of a logical or mathematical expression. In this case variable, is referred to in the course of coding and decoding. The method of coding and decoding could vary, as described in applicant's specification, for example in page 25, lines 29-35, "In this embodiment, --- theory.".

The purpose of "Invalid bit":

The term "invalid bit" is meant as a "padding bit". Claims 6 and 7 are amended for clarity. Support for these features is described in applicant's specification, for example in page 27, line 31 through page 28, line 15 and Fig. 8.

The claim amendments are to clarify the features as pointed out by the claim objections. The claims have not been narrowed. No new matter is entered.

Claim Rejections

Claims 1 and 2 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Titchener (U.S. 4,670,890) in view of Ramesh et al. (U.S. 6,275,538) (Ramesh).

Titchener describes a method and means for creating a fixed length depleted code for use in digital processors and digital storage media. Titchener does not show the details of the logical operations on a combination of logic values. The Office Action relies on Ramesh to show this feature.

However, it is respectfully submitted that claims 1 and 2 cannot be rendered obvious in view of the cited references of the following reasons:

One of the characteristics of the inventions of claims 1 and 2 is that coding or decoding is done by repeatedly performing logical operations on the object of operation and the argument (variable), through the combination circuit.

In particular Claim 1 recites holding an argument that should be applied to an operation that is performed on a word that is subsequently held by said operating-object holding means, and the argument being included in said word being held by said operating-object holding means and/or the result of an operation performed in advance on the word being held by said operating-object holding means; and

performing, as said operation, in accordance with logical values of individual bits that are included in said word being held by said operating-object holding means and said argument being held by said argument holding means, coding that is defined as a logical operation to be performed on a combination of said logical values.

The object of operation here is input in divisions and comprised of a plurality of bits, and the argument here is an argument (variable), which is to be applied to the operation to be done in advance on the word.

In contrast to the claimed invention, the configurations taught by Titchener and Ramesh are different from claims 1 and 2 because, in part, Titchener fails to show details of the logical operations on a combination of logic values and Ramesh does not disclose the shifting and operations being performed on units of words each comprised of a plurality of bits, as follows:

One main characteristics of Titchener is the invention is used for transmitting sequential information as an indefinite length string of data, and the code symbols are automatically synchronized so that coding is sufficiently accomplished even for a simple coding process.

In Ramesh there is a convolutional feedback encoder having a shift register which encodes a fixed length information sequence, and which has a feed-forward circuit and a feedback circuit.

However, Ramesh only discloses a convolutional feedback encoder as a "logic circuit" that performs shifting and predetermined operations on a single bit input or passed over in series, in a time sequence. Ramesh does not disclose the shifting and operations being performed on units of words each comprised of a plurality of bits, as in the present invention.

For example applicant's claim 1 recites: holding an argument that should be applied to an operation that is performed on a word that is subsequently held by said operating-object holding means.

Moreover, in Ramesh, the shifting and the operations stated above are performed not in units of words, but in units of single bits, by a sequential circuit, which is essentially different from the combination circuit in the present invention as provided in the claims.

Furthermore, applicant's claims provide an operation realizing convolutional encoding and other encoding to be done in units of words which each consist of plural bits. This is neither suggested nor disclosed by the combination of Tichener and Ramesh. Neither the object of

operation to be referred to in the course of operation on units of words of plural bits, nor arguments to be passed over during the operation subsequently performed, are disclosed in connection to methods and forms of coding (encoding) in Tichener or Ramesh et al.

Therefore it is respectfully submitted neither of the inventions recited in claims 1 or 2 are obvious from the combination of Titchener and Ramesh.

Further applicant claims a unique combination of features in claims 1 and 2 that provide unique results that cannot be achieved by the combination of Tichener and Ramesh because of the differences in configurations. Applicant's specification provides evidence of these results from the unique combination of elements as the following:

p. 7, lines 25-28 "which can realize desired coding ... to a large extent"; and

p. 8, lines 17-25 "to increase the service quality ... call setting procedure.".

It is well-established that a combination of limitations, some of which separately may be known, may be a new combination of limitations which is nonobvious under the condition of 35 U.S.C. 103. Moreover, "an examiner may often find every element of a claimed invention in the prior art." In re Rouffet, 47 USPQ3d 1453, 1457 (Fed. Cir. 1998) (reversing PTO obviousness rejection based on lack of suggestion or motivation to combine reference). Therefore even if every element of a claimed invention is in the combined prior art there must be some suggestion or motivation to combine the references. "Although a reference need not expressly teach that the disclosure contained therein should be combined with another, the showing of combinability, in whatever form must nevertheless be 'clear and particularity.'" In re Dembiscak, 175 F.3d 994, 999 (CAFC 1999).

The only such suggestion provided has been from applicant's own disclosure.

Claims 3-6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Titchener in view of Ramesh and with regard to claims 3 and 4 further in view of Lan et al. (U.S. 5,787,099). Claim 5 is rejected further in view of Kindred et al. (U.S. 5,710,784) and claim 6 is rejected further in view of Kim (U.S. 5,162,908).

With regard to claims 3-6, it is respectfully submitted that dependent claims 3-6 are in condition for allowance since the combination of Titchener, Ramesh and any of Lan et al., Kindred et al., or Kim shows the features of Applicant's claims 1 or 2. Further these dependent claims provide additional features over claims 1 and 2. For at least the reasons stated above these claims should be allowed.

Claims 7-14 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Titchener in view of Ramesh and further in view of Sugahara et al. (U.S. 6,483,944) (Sugahara).

It is respectfully submitted that dependent claims 7-14 are in condition for allowance since the combination of Titchener, Ramesh in view of Sugahara does not teach the distinguishing feature of claims 1 or 2 and further claims 7-14 contain additional distinguishing features.

Claims 15 and 16 are unpatentable over Titchener in view of Ramesh and further in view of Astrachan (U.S. 5,612,974).

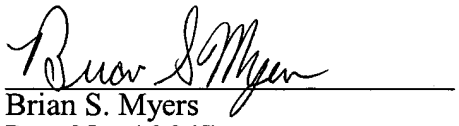
However, claims 15 and 16 contain similar distinguishing features as claims 1 and 2 and would likewise not be obvious in view of the cited references Tichener and Ramesh since the cited Astrachan does not teach the deficiencies of Tichener and Ramesh.

In view of the remarks set forth above, this application is in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider

this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,



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